19-2987; Rev 0; 9/03

MAXIM

225MHz, Triple, 2-Channel Video Multiplexer-Amplifier

General Description

The MAX4027 is a triple, wideband, 2-channel, noninverting gain-of-two video amplifier with input multiplexing, capable of driving up to two back-terminated video loads. The MAX4027 features current-mode feedback amplifiers configured for a gain of two (+6dB) with a -3dB large-signal bandwidth of 200MHz. The device has low (0.012%/0.014°) differential gain and phase errors, and operates from ±5V supplies.

The MAX4027 is ideal for use in broadcast and graphics video systems because of the low 2pF input capacitance, channel-to-channel switching time of only 15ns, and wide 62MHz, large-signal 0.1dB bandwidth. High-impedance output disabling allows the MAX4027 to be incorporated into large switching arrays with minimal interaction with the source. Specified over the -40°C to +85°C extended temperature range, the MAX4027 is available in 14-pin SO and TSSOP packages.

Applications

Video Source Selection (Multiplexing)

Picture in Picture (PIP) Insertion

Crosspoint Expansion

Coaxial Cable Drivers

Supports VGA to UXGA (1600 x 1200) Resolution

Enterprise Class (Blade) Servers

Keyboard-Video-Mouse (KVM)

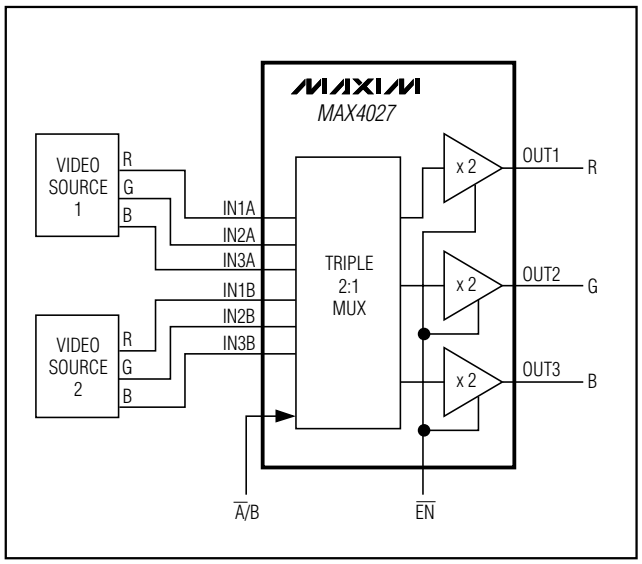
Features

- **Excellent Video Specifications:**
  - **75MHz Small-Signal 0.1dB Gain Flatness**
  - **62MHz Large-Signal 0.1dB Gain Flatness**
  - **0.012%/0.014° Differential Gain/Phase Error**
- **VGA to UXGA Resolution**
- **High Speed:**
  - **200MHz $2V_{P-P}$ -3dB Bandwidth**
  - **1100V/µs Slew Rate**
  - **15ns Settling Time to 0.1%**
- **Internal Gain of 2V/V Compensates for Output Back Termination**
- **Fast Switching:**
  - **15ns Channel-Switching Time**
  - **260mV_{P-P} Switching Transient**
- **Drives Two Back-Terminated Video Loads**
- **High-Impedance Output Disable**

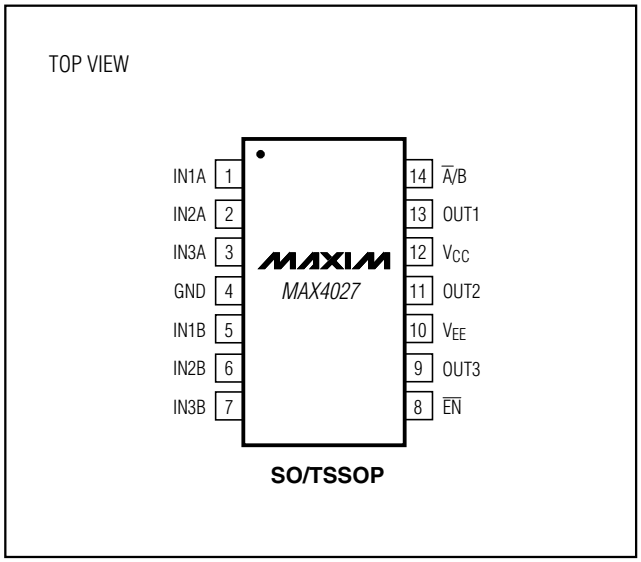
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4027ESD	-40°C to +85°C	14 SO
MAX4027EUD	-40°C to +85°C	14 TSSOP

Typical Operating Circuit



Pin Configuration



225MHz, Triple, 2-Channel Video Multiplexer-Amplifier

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC} to GND) .....+6V
Negative Supply Voltage (V_{EE} to GND) .....-6V
Amplifier Input Voltage (IN_ _) .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage ($\overline{EN}$, $\overline{A}$/B) .....-0.3V to (V_{CC} + 0.3V)
Output Short Circuit to GND (Note 1) .....Continuous
Output Short Circuit to V_{CC} or V_{EE} 5s

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
14-Pin SO (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Continuous power-dissipation rating must also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, $V_{IN\_\_}$ = 0V, R_L = 150Ω to GND, T_A = -40°C to +85°C. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Inferred from the PSRR test		+4.5	+5.0	+5.5	V
	V_{EE}			-4.5	-5.0	-5.5	
Positive Supply Current	I_{CC}	$\overline{EN}$ = GND			31	39	mA
		$\overline{EN}$ = 5V			17	24	
Negative Supply Current	I_{EE}	$\overline{EN}$ = GND			28	36	mA
		$\overline{EN}$ = 5V			15	21	
Input Voltage Range	$V_{IN\_\_}$	Inferred from voltage gain		±1.25	±1.75		V
Input Offset Voltage	V_{OS}	T_A = +25°C			±1	±6	mV
		T_A = -40°C to +85°C				±11	
Input Offset-Voltage Matching	ΔV_{OS}	Channel to channel			±1	±12	mV
Voltage Gain	A_V	$V_{OUT\_}$ = ±2.5V		1.9	2.0	2.1	V/V
Input Offset-Voltage Temperature Coefficient	TCV_{OS}				1		µV/°C
Input Bias Current	I_B	T_A = +25°C			±2	±10	µA
		T_A = -40°C to +85°C				±18	
Input Resistance	R_{IN}	$V_{IN\_\_}$ = -1.25V to +1.25V	Channel on	100	400		kΩ
			Channel off	1	20		MΩ
DC Output Resistance	R_{OUT}				10		mΩ
Disabled Output Resistance	$R_{OUT(d)}$	$\overline{EN}$ = 5V, $V_{OUT\_}$ = -2.5V to +2.5V (Note 3)			1.6		kΩ
DC Power-Supply Rejection Ratio	PSRR	V_{CC} = +4.5V to +5.5V, V_{EE} = -4.5V to -5.5V		60	86		dB
Output Voltage Swing	$V_{OUT\_}$			±2.5	±3.5		V
Output Short-Circuit Current	I_{SC}				±143		mA
LOGIC CHARACTERISTICS ($\overline{EN}$, $\overline{A}$/B)							
Logic-Low Threshold	V_{IL}					0.8	V
Logic-High Threshold	V_{IH}			2.0			V
Logic-Low Input Current	I_{IL}	V_{IL} = 0V			-4	-20	µA
Logic-High Input Current	I_{IH}	V_{IH} = +5.5V, V_{CC} = +5.5V			350	600	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5V, $V_{IN\_\_}$ = 0V, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS						
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{IN\_\_}$ = 20mV_{P-P}		225		MHz
Small-Signal Bandwidth for ±0.1dB Gain Flatness	$BW_{LS(0.1)}$	$V_{IN\_\_}$ = 20mV_{P-P}		75		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{IN\_\_}$ = 1V_{P-P}		200		MHz
Large-Signal Bandwidth for ±0.1dB Gain Flatness	$BW_{LS(0.1)}$	$V_{IN\_\_}$ = 1V_{P-P}		62		MHz
Slew Rate	SR	$V_{IN\_\_}$ = 1V_{P-P}		1100		V/µs
Settling Time to 0.1%	t_S	$V_{IN\_\_}$ = 1V_{P-P}		15		ns
Differential Gain Error	DG	5-step modulated staircase (Note 4)		0.012		%
Differential Phase Error	DP	5-step modulated staircase (Note 4)		0.014		degrees
Delay Between Channels	t_D	$V_{IN\_\_}$ = 1V_{P-P}, t_R = 100ps		0.1		ns
Channel-to-Channel Crosstalk	X_{TALK}	$V_{IN\_\_}$ = ±1V_{P-P}, f = 10MHz		-61		dB
$\overline{A}$/B Crosstalk		$V_{IN\_\_}$ = ±1V_{P-P}, f = 10MHz		-80		dB
Output Impedance	Z_{OUT}	f = 10MHz		1		Ω
Total Harmonic Distortion	THD	$V_{OUT\_}$ = 2V_{P-P}, f = 10MHz		64		dBc
Off-Isolation	A_{ISO}	$V_{OUT\_}$ = 2V_{P-P}, f = 10MHz, R_S = 75Ω		-83		dB
Output Capacitance	C_{OUT}	Channel on or off		3		pF
Input Capacitance	C_{IN}	Channel on or off		2		pF
Input-Voltage Noise Density	e_n	f = 100kHz		6.5		nV/√Hz
Input-Current Noise Density	i_n	f = 100kHz		6.5		pA/√Hz
SWITCHING CHARACTERISTICS						
Channel-Switching Time	t_{SW}	(Notes 5, 6)		15		ns
Enable Delay Time	t_{PDE}	(Notes 5, 7)		20		ns
Disable Delay Time	t_{PDD}	(Notes 5, 7)		25		ns
Switching Transient	V_{TRAN}	(Note 8)		260		mV_{P-P}

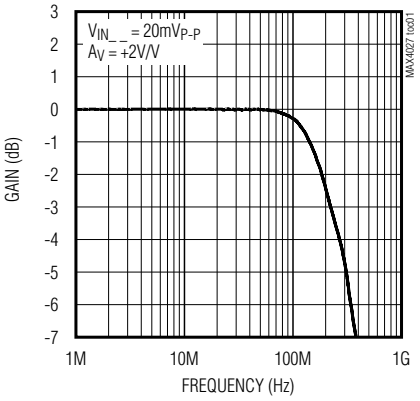
Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: Disabled output resistance includes the internal feedback network.
Note 4: Input test signal is NTSC composite with 5-step staircase, of 40 IRE per step, modulated with 3.58MHz color subcarrier.
Note 5: See the Timing Diagram (Figure 2).
Note 6: Channel-switching time specified for switching between input channels; does not include signal rise/fall times for switching between channels with different input voltages.
Note 7: Output enable/disable delay times do not include amplifier output slewing times.
Note 8: Switching transient measured while switching between two grounded channels.

225MHz, Triple, 2-Channel Video Multiplexer-Amplifier

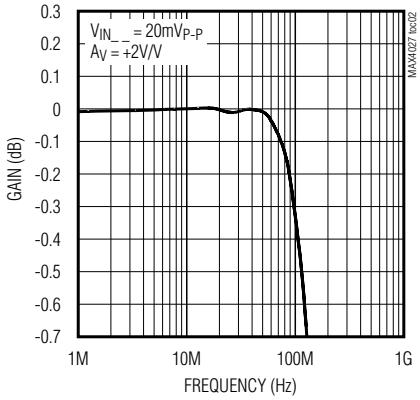
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise noted.)

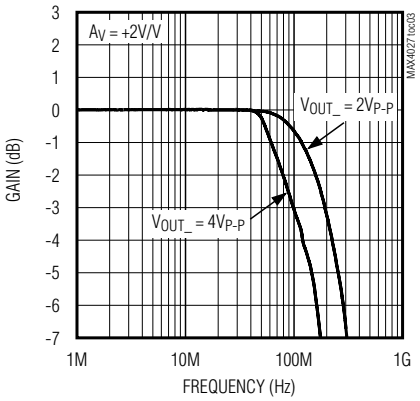
SMALL-SIGNAL FREQUENCY RESPONSE



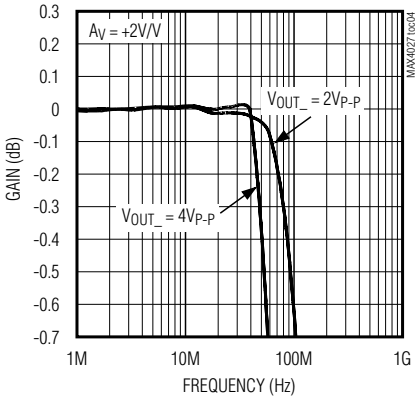
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



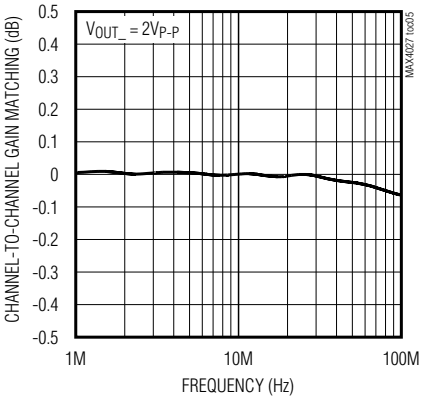
LARGE-SIGNAL FREQUENCY RESPONSE



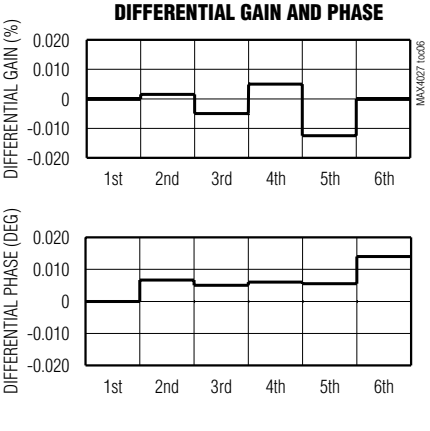
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



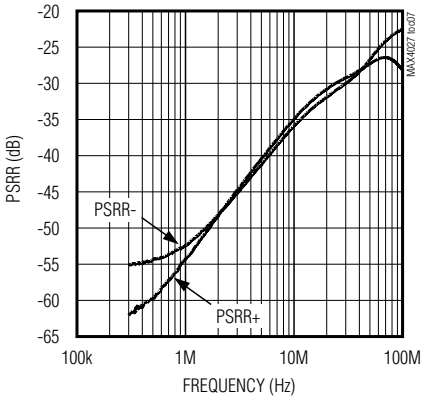
CHANNEL-TO-CHANNEL GAIN MATCHING vs. FREQUENCY



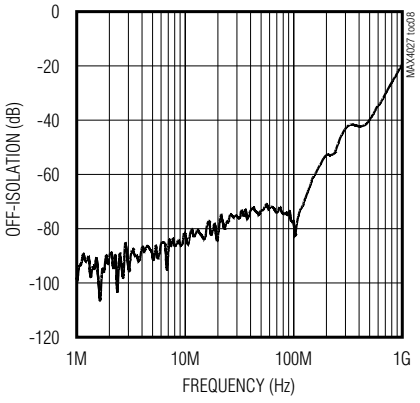
DIFFERENTIAL GAIN AND PHASE



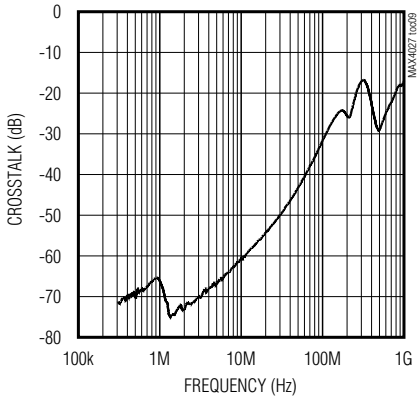
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OFF-ISOLATION vs. FREQUENCY



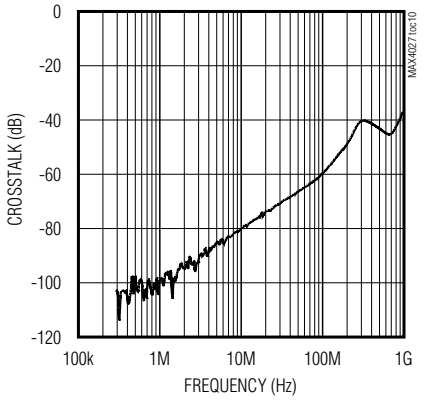
CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



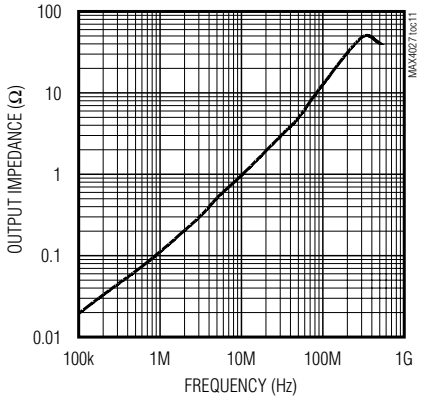
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise noted.)

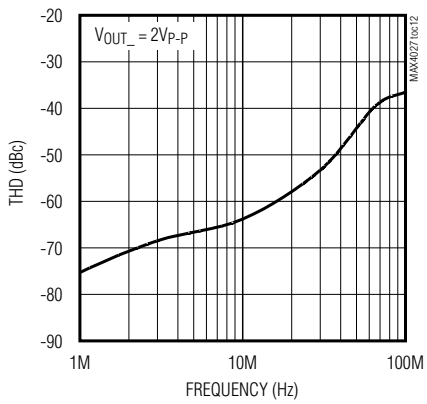
Ā/B CROSSTALK vs. FREQUENCY



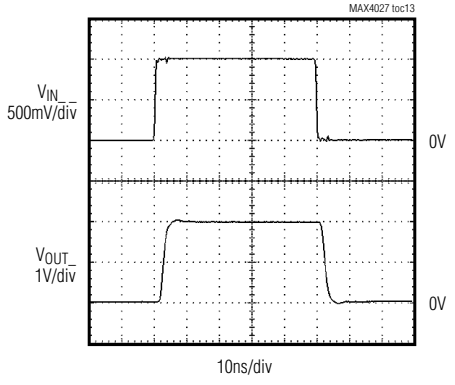
OUTPUT IMPEDANCE vs. FREQUENCY



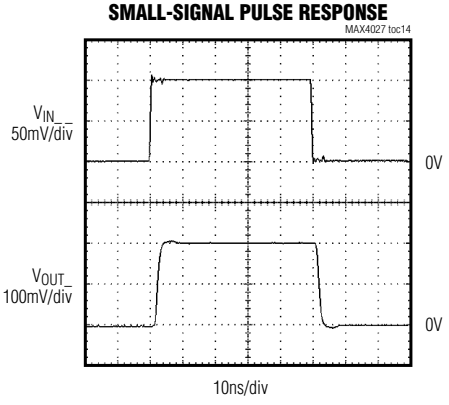
TOTAL HARMONIC DISTORTION vs. FREQUENCY



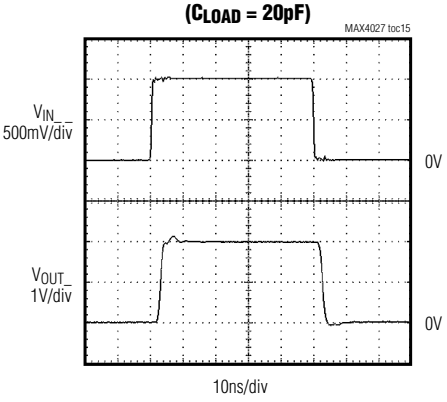
LARGE-SIGNAL PULSE RESPONSE



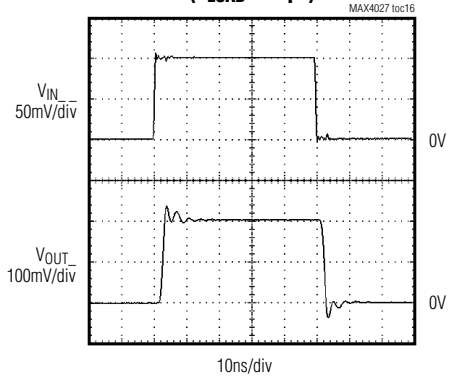
SMALL-SIGNAL PULSE RESPONSE



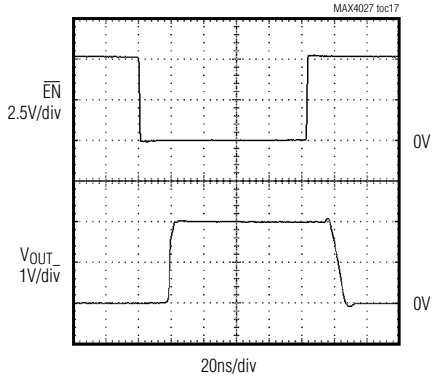
LARGE-SIGNAL PULSE RESPONSE (C_{LOAD} = 20pF)



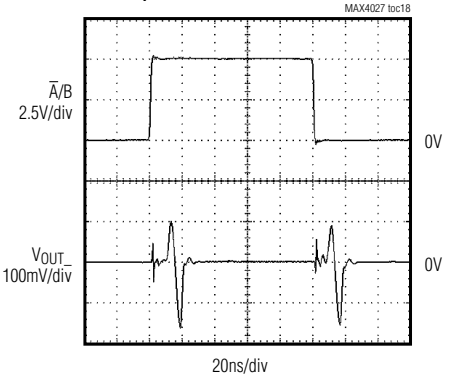
SMALL-SIGNAL PULSE RESPONSE (C_{LOAD} = 20pF)



ENABLE RESPONSE TIME



A/B SWITCHING TRANSIENT



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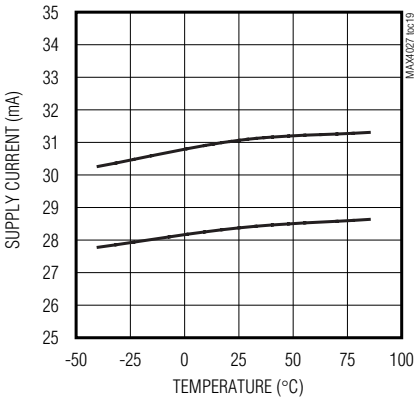
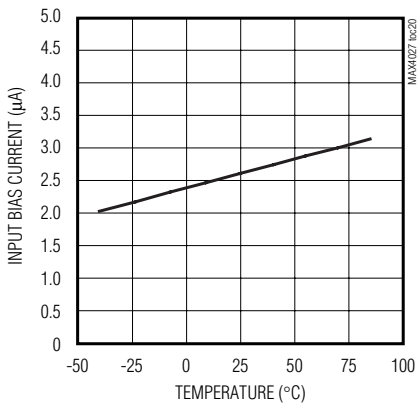
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise noted.)

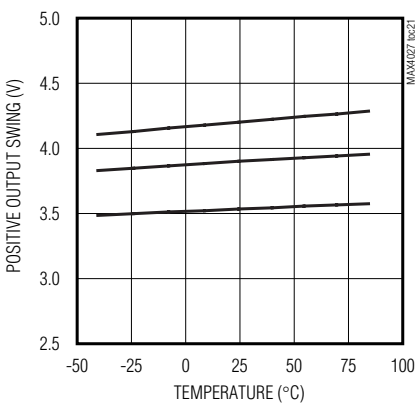
SUPPLY CURRENT vs. TEMPERATURE



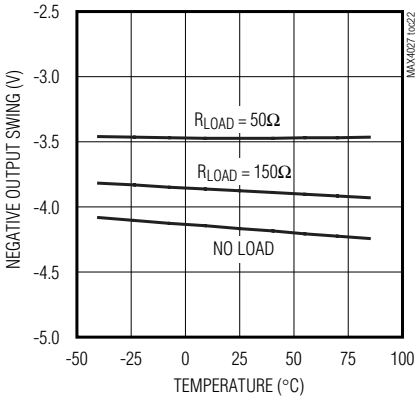
INPUT BIAS CURRENT vs. TEMPERATURE



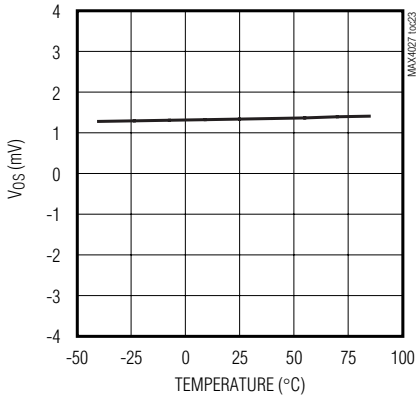
POSITIVE OUTPUT SWING vs. TEMPERATURE



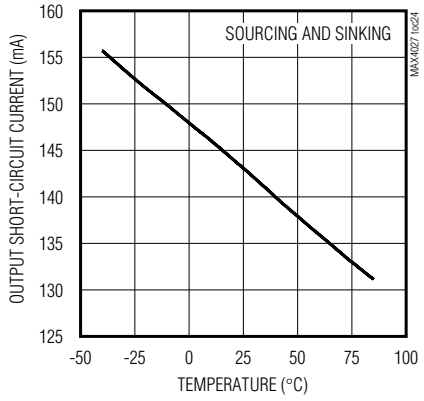
NEGATIVE OUTPUT SWING vs. TEMPERATURE



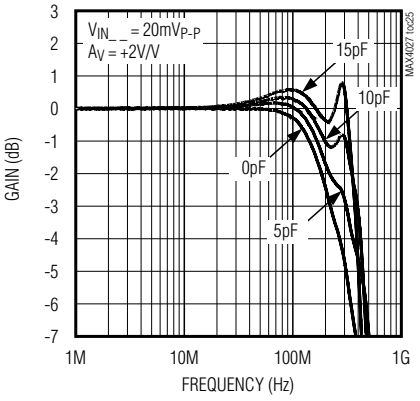
INPUT OFFSET VOLTAGE vs. TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE



SMALL-SIGNAL BANDWIDTH vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	IN1A	Amplifier 1 Channel A Input
2	IN2A	Amplifier 2 Channel A Input
3	IN3A	Amplifier 3 Channel A Input
4	GND	Power Supply, Analog and Digital Ground. Connect GND to ground plane for best RF performance.
5	IN1B	Amplifier 1 Channel B Input
6	IN2B	Amplifier 2 Channel B Input
7	IN3B	Amplifier 3 Channel B Input
8	$\overline{EN}$	Output Enable Logic Input. Drive $\overline{EN}$ low or leave open for normal operation. Pull $\overline{EN}$ high to disconnect amplifier output (output is high impedance when disabled). $\overline{EN}$ is internally pulled to GND through a 17kΩ resistor.
9	OUT3	Amplifier Output 3
10	V_{EE}	Negative Power-Supply Voltage. Bypass V_{EE} to GND with a 0.1µF capacitor.
11	OUT2	Amplifier Output 2
12	V_{CC}	Positive Power-Supply Voltage. Bypass V_{CC} to GND with a 0.1µF capacitor.
13	OUT1	Amplifier Output 1
14	$\overline{A}$/B	Channel-Select Input. Drive $\overline{A}$/B low or leave open to select channel A for all amplifiers. Pull $\overline{A}$/B high to select channel B for all amplifiers. $\overline{A}$/B is internally pulled to GND through a 17kΩ resistor.

Detailed Description

The MAX4027 combines three 2:1 multiplexers with +2V/V (+6dB) closed-loop gain (A_{VCL}) amplifiers. This low-power, high-speed device operates from ±5V supplies, while driving up to two back-terminated video loads with very low distortion. Differential gain and phase errors are 0.012%/0.014° for the MAX4027.

The input multiplexers feature fast 15ns channel-switching times and small switching transients. The multiplexers also feature high input resistance and constant input capacitance, so overall input impedance can be set by external input-terminating resistors.

Drive $\overline{EN}$ high to place the amplifier outputs in a high-impedance state, and minimize the supply current. This function allows use of multiple mux/amps in parallel to form large switching arrays.

The MAX4027 features an $\overline{A}$/B input, which selects either channel A or B. Drive $\overline{A}$/B low to select channel A or drive $\overline{A}$/B high to select channel B. Channel A is automatically selected if $\overline{A}$/B is left unconnected.

Truth Tables

Table 1. Input Control Logic

$\overline{A}$/B	AMPLIFIER INPUT	FUNCTION
0	IN_A	Channel A Selected
1	IN_B	Channel B Selected

Table 2. Output Control Logic

$\overline{EN}$	AMPLIFIER OUTPUT	FUNCTION
0	On	Outputs Enabled
1	Off	Outputs High Impedance

Applications Information

Disable Mode

Drive $\overline{EN}$ high to place the MAX4027 in disable mode. Placing the device in disable mode reduces the quiescent current to 17mA (V_{CC}) and 15mA (V_{EE}) and places the amplifier outputs into a high-impedance state, typi-

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cally 1.6kΩ. Parallel multiple devices to construct larger switch matrices by connecting the outputs of several devices together and disabling all but one of the paralleled amplifiers' outputs. Two internal 800Ω thin-film resistors set the MAX4027 to a fixed gain of +2. Consider the impedance of the internal feedback resistors when operating multiple MAX4027s in large multiplexer applications.

Drive $\overline{EN}$ low for normal operation. $\overline{EN}$ has internal pull-down circuitry. The MAX4027 is enabled when $\overline{EN}$ is unconnected.

Video Line Driver

The MAX4027 is well suited to drive short coaxial transmission lines when the cable is terminated at both ends (Figure 1) where the fixed gain of +2 compensates for the loss in the back termination. Cable frequency response may cause variations in the flatness of the signal.

Input Voltage Range

The guaranteed input voltage range is ±1.25V. Exceeding this value can cause unpredictable results, including output clipping, excessive input current, and switching delays.

Multiplexer

The input multiplexer (mux) is controlled by a 3.3V TTL/CMOS-compatible control input (see the *Truth Tables*). Input capacitance is a constant, low 2pF and input resistance is 17kΩ to GND for all input channels, regardless of whether or not the channel is selected. All logic levels ($\overline{EN}$ and $\overline{A}$/B) default low if left unconnected.

Layout and Power-Supply Bypassing

The MAX4027 has an extremely high bandwidth and requires careful board layout. For best performance, use constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on an internal layer that incorporates no signal or power traces.

Observe the following guidelines when designing the board regardless of whether or not a constant-impedance board is used.

1) Do not use wire-wrap boards or breadboards.
2) Do not use IC sockets; they increase parasitic capacitance and inductance.
3) Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.
4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
5) Use surface-mount components. They generally have shorter bodies and lower parasitic reactance, yielding better high-frequency performance than through-hole components.

The bypass capacitors should include a 0.1µF ceramic surface-mount capacitor between each supply pin and the ground plane, located as close to the package as

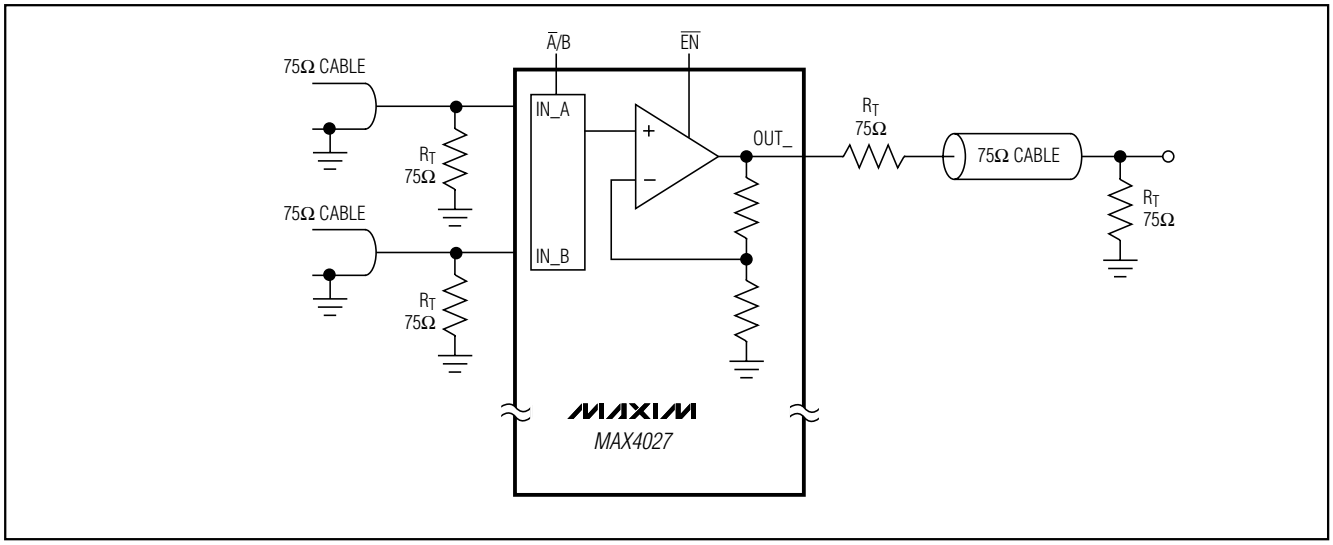


Figure 1. Video Line Driver

possible. Optionally, place a 10µF tantalum capacitor at the power-supply pins' points of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins.

Use surface-mount resistors for input termination and output back termination. Place the termination resistors as close to the IC as possible.

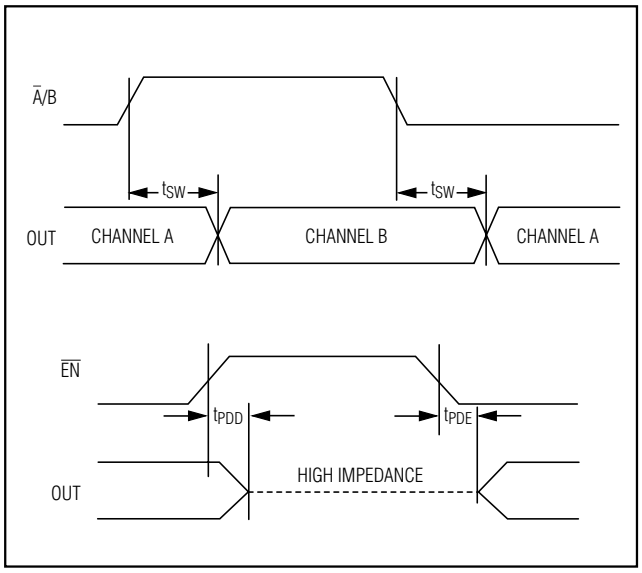
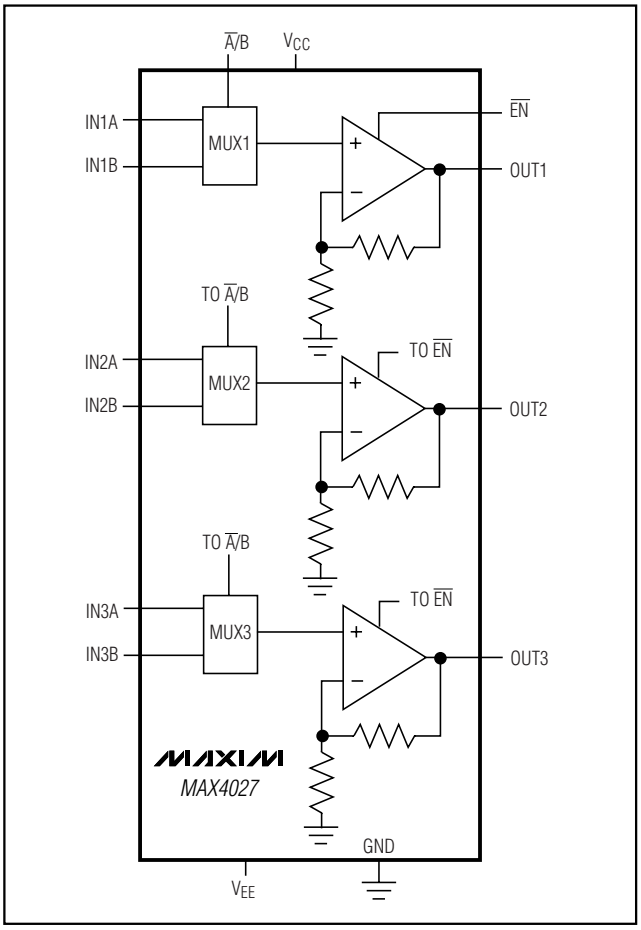


Figure 2. Switching Timing Diagram

Functional Diagram



Chip Information

TRANSISTOR COUNT: 870

PROCESS: Bipolar

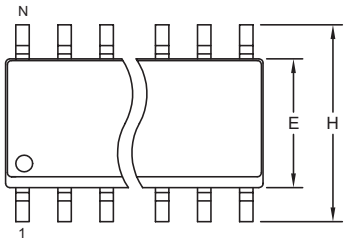
225MHz, Triple, 2-Channel Video Multiplexer-Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

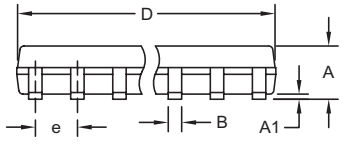
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



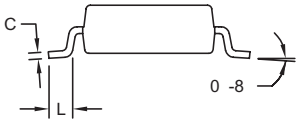
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

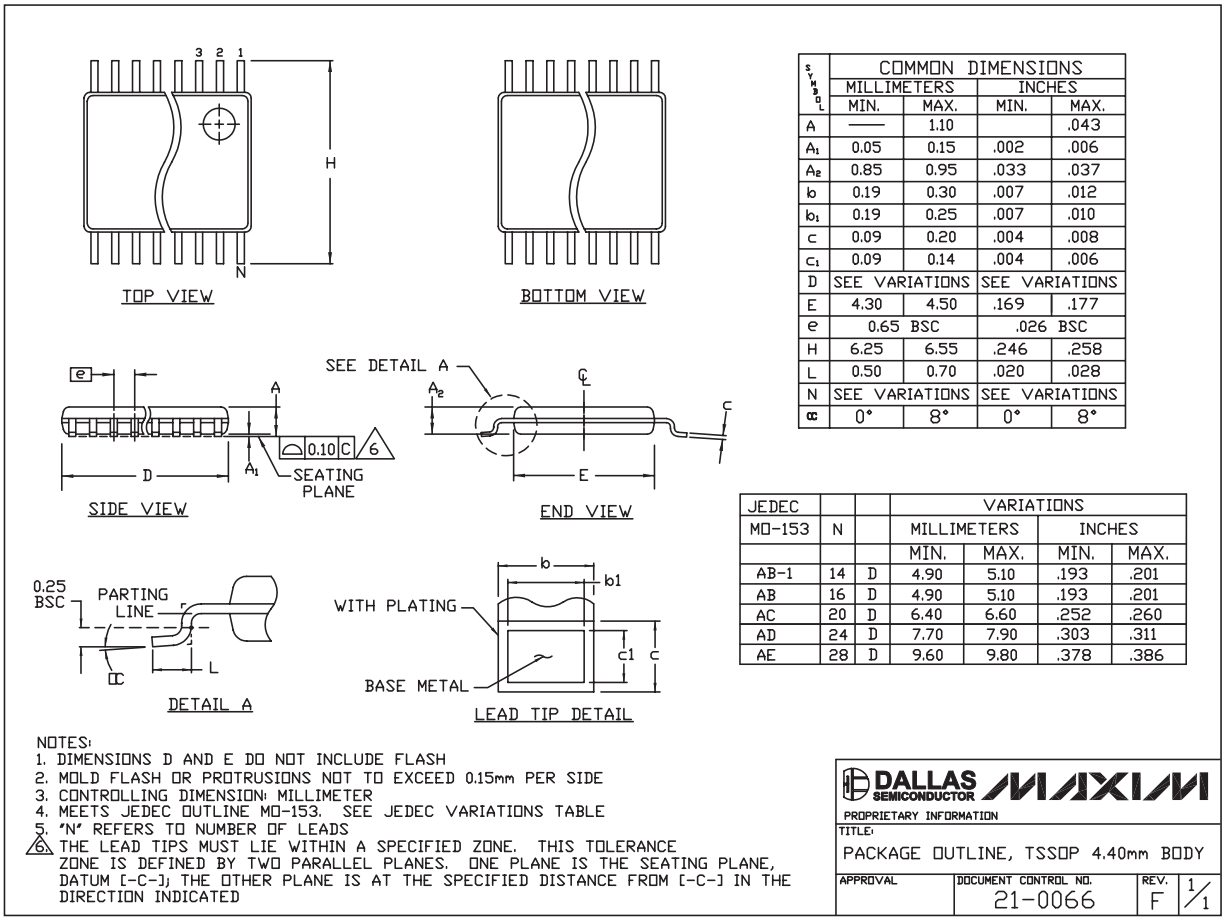
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1